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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,496	11/09/2001	Fong Piau	FLEX1814	3412

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	11

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/053,496	Applicant(s) PIAU ET AL.	
	Examiner Midys Inoa	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 2003/0009607 A1) in view of Katayama et al. (US 2001/0007119 A1) and further in view of Chien et al. (US 2003/0033465 A1).

Regarding Claim 1, 9, and 17 Chen teaches a flash system that is controlled by a flash controller 204 in which the controller controls and initiates the functionality of the system components, processes a series of commands such as write or read, and executes transfers of data from and to the flash ROM (Page 3, paragraphs 0028-0030). Chen does not teach a flash memory comprising of a number of flash memory arrays, the partitioning of the flash memory arrays, or the transfer of data to a memory array pair. Katayama et al. teaches a file memory device comprising a flash memory 5 with a number of memory arrays (Figure 3). The memory arrays of Katayama are organized in a parallel arrangement of memory element groups ("partitioning flash memory arrays"). In addition, the data being transferred is distributed through out the arrays through the use of a data distribution unit within the data control circuit. In the case where the flash memory were to be divided into only two memory arrays, the **data distribution unit would serve the purpose of transferring data to a memory array pair**. Such a scenario is explored in Figure 11 where the distribution of data for two memory groups

(or memory arrays) is explored (Paragraph 101). The memory groups "a" and "b" are those memory arrays that make up the memory array pair. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the flash memory partitioning and data transferring method of Katayama et al. with the system of Chen in order to give the system the added ability of interleaving data throughout the memory arrays, thus making the transfer of data faster. The combination of Chen and Katayama et al. does not disclose a flash controller configured to partition the flash memory arrays in accordance to the parameters of a configuration information table stored in a memory of the compact flash controller. Chien et al. discloses an IDE system in which an IDE controller 10 comprises a memory 10a and reads from its memory a **partition table ("configuration information table") and provides information from this table** to the ATA interface **in order to create virtual partitions in the disk drive device** 30 (Paragraphs 19 and 22). Chien discloses that the real disk drive device could be a flash memory storage device (Claim 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the partitioning table of Chien et al. with the combined system of Chen and Katayama et al. since it would allow for the flash memory system to work not only in memories that have been partitioned in hardware, but also in non partitioned memories which could later be partitioned virtually by the controller.

Regarding Claims 2-3, 10-11, and 18-19, Chen teaches a system in which there is a choice as to what interface to use for the movement of data. When the system is in a flash ROM programming mode, an IDE interface is used. When the system is dealing with task files, an ATA interface is in effect ("an ATA or IDE interface is selected", Page 2, paragraph 0019).

Regarding Claims 4,12 and 20, Chen teaches a system in which the host provides the flash controller with a write command (specified command sequence) which is interpreted by the controller (data transfer operative elements) and allows it to perform the necessary steps to write data from the controller into the flash ROM, thus completing the data transfer operation (Page 3, paragraph 0030).

Regarding Claims 5, 13 and 21, Chen teaches a system in which the host provides the flash controller with a read command (specified command sequence) which is interpreted by the controller (data transfer operative elements) and allows it to perform the necessary steps to read data from the flash ROM and store it in a RAM that is accessible to the host, thus completing the data transfer operation (Page 3, paragraph 0031).

Regarding Claims 6, 14, and 22, Chen teaches a system in which a "LENGTH" register specifies the number of bytes that need to be transferred, thus allowing the flash controller to continue the transfer operation until the system receives or transfers the specified number of bytes. This is how the controller knows that the operation has been completed (Page 3, paragraph 003, lines 15-16 and paragraph 0031, lines 8-9).

Regarding Claims 7-8, 15-16, and 23-24, Chen's flash controller does not perform any write, read, or transfer operation until a command is received from the host. Therefore, essentially, the flash controller stops operation and waits for a request from the host before is resumes normal operation.

Response to Arguments

3. Applicant's arguments filed on March 8th, 2004 with respect to claims 1, 9 and 17 have been considered but are moot in view of the new ground(s) of rejection.

The reference of Chien et al. teaches the elements not taught by Chen in view of Katayama. Katayama et al. teaches a file memory device comprising a flash memory divided into memory arrays (Figure 3). The memory arrays of the flash memory are organized in a parallel arrangement of memory element groups, which in turn constitute a form of memory array partitioning. The data being transferred in Katayama's system is distributed through out the arrays through the use of a data distribution unit, which, in the case where the flash memory were to be divided into only two memory arrays, the **data distribution unit would serve the purpose of transferring data to a memory array pair** (Figure 11). Although Katayama does discloses the transfer of 32 bit data in parallel groups of four 8 bit blocks to four memory chips in Figures 8 and 10; **for the rejection of Claims 1, 9, and 17, the Examiner is referring to the teachings of Figure 11** where Katayama teaches a **control data distribution through out two memory groups or two flash memory arrays**. The memory control circuit 28 controls the flash memory 5, however, it does not control the partitioning of the flash memory. Chien et al. discloses an IDE **controller, which stores in its memory a partitioning table used to create virtual partitions in memory**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
Examiner
Art Unit 2188

MI

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